SHIRDI SAI ENGG COLLEGE

2002 SCHEME

USN | | | | | | | | | | |

EC74

Seventh Semester B.E. Degree Examination, June 2012
VLSI Circuits

Time: 3 hrs. Max. Marks:100

Note: ***1. Answer any FIVE full questions.***
2. Assume typical device parameter values, if necessary.

Important Note : 1. On completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages.
2. Any revealing of identification, appeal to evaluator and /or equations written eg, 42+8 = 50, will be treated as malpractice.

1 a. Using the flowchart, explain the "Top down" and "Bottom up" approach in VLSI design. **(05 Marks)**

b. Explain the complexity of VLSI chip using the idea of VLSI design funnel. **(05 Marks)**

c. Explain the concept of bubble pushing to build the PFET array of MOSFET circuit. Using this technique construct the CMOS logic gate for the function $g = \overline{x \cdot (y+z) + y}$. Use minimum transistors in the design. **(10 Marks)**

2 a. Discuss the pass characteristics of nFETs. Show that nFETs pass strong logic zero voltages but weak logic 1 values. **(06 Marks)**

b. Consider the three MOSFETs connected as shown in Fig.Q2(b). Find V_{out} for the following values of V_a, V_b and V_c. Assume $V_{DD} = 3.3V$, $V_{Tn} = 0.6V$.

i) $V_a = 3.3V$, $V_b = 3.3V$, $V_c = 3.3V$

ii) $V_a = 3V$, $V_b = 0.5V$, $V_c = 3V$

iii) $V_a = 3.3V$, $V_b = 1.8V$, $V_c = 1.5V$

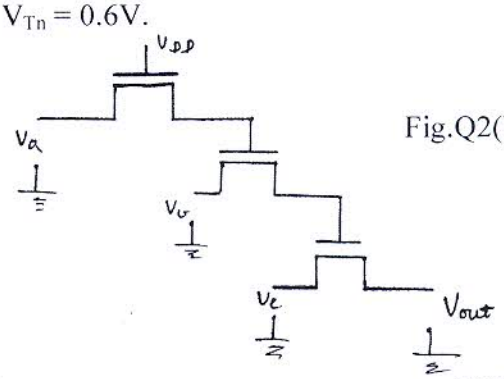

Fig.Q2(b)

(06 Marks)

c. Design 4:1 multiplexer using transmission gate switches. **(08 Marks)**

3 a. With the cross-sectional schematic view of a N well CMOS process. Identify various layers. **(04 Marks)**

b. A sample of silicon is doped with boron atoms at an acceptor density of $N_a = 4 \times 10^{14}\ cm^{-3}$

i) Find majority and minority carrier densities.

ii) Find the resistivity ρ of the sample.

iii) Suppose the region has dimensions of W = 2μm, t = 0.5μm and L = 100μm. Find resistance of end to end block of the region. **(06 Marks)**

c. Design the circuit and layout for a CMOS gate that implements the function, $F = \overline{a \cdot bc + a \cdot d}$, using fewest number of transistors. **(10 Marks)**

4 a. Explain the latch up prevention in a bulk CMOS technology. **(08 Marks)**

b. With cross-sectional view illustrate the use of a via to connect metal1 to metal2. Draw the layout including design rule. **(06 Marks)**

c. Implement symmetric inverter with vertical FETs. Explain with neat layout. **(06 Marks)**

5 a. Derive expression for rise time and fall time for a CMOS inverter circuit. **(08 Marks)**

b. Consider the NOT gate shown in Fig.Q5(b). When an external load of C_L = 80 fF is connected to output, find i) the input capacitance of the circuit ii) Values of R_n and R_p iii) Calculate rise and fall times for the inverter. **(12 Marks)**

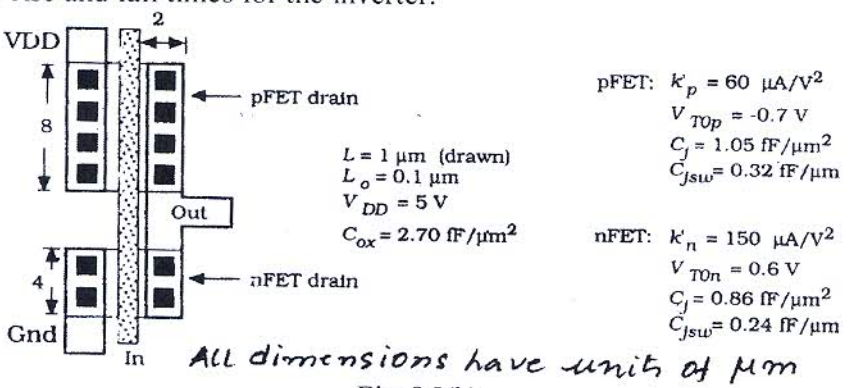

Fig.Q5(b)

6 a. Explain speed versus area trade off in chip design. **(06 Marks)**

b. Consider nFET chain as in Fig.Q6(b). The transistors are identical with $\beta_n = 2.0$ mA/V^2 in a process where $V_{DD} = 3.3$V, $V_{Tn} = 0.7$V. The output capacitance has value of $C_{out} = 130$fF, while the internal values are $C_1 = 36$ fF and $C_2 = 36$ fF.

i) Find the discharge time constant using the Elmore formula for RC ladder network for $C_{out} = 130$ fF.

ii) Find the time constant if we ignore C_1 and C_2 , what is the percentage error introduced if we do not include the internal capacitors? **(06 Marks)**

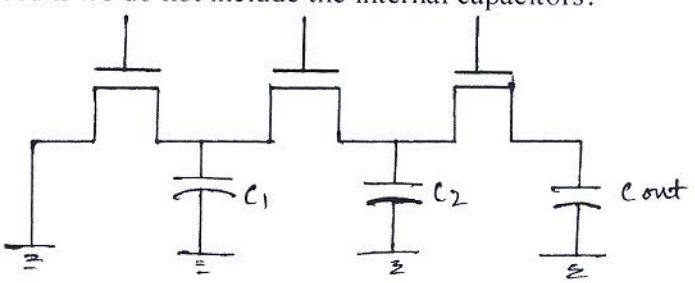

Fig.Q6(b)

c. Explain NOR2 switching times. **(08 Marks)**

7 a. Construct a BiCMOS NOR2 circuit. **(08 Marks)**

b. Define i) Logical effort ii) Electrical effort.

The long chain in Fig.Q7(b) is constructed in a process with r = 2.5. Determine the optimum sizing for each stage for the "highlighted" path indicated using the technique of logical effort. **(12 Marks)**

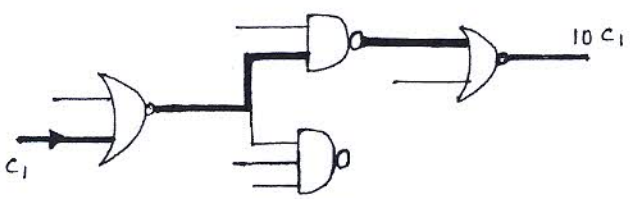

Fig.Q7(b)

8 a. Explain the pseudo nMOS logic. **(05 Marks)**

b. Draw the circuit diagram for dynamic logic gate that has an output of $f = \overline{a \cdot (b + c + d)}$. **(05 Marks)**

c. Compare blocked CMOS circuits with dynamic CMOS logic circuits, with neat diagrams and examples. **(10 Marks)**

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