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Seventh Semester B.E. Degree Examination, Dec.2013/Jan.2014

Embedded System Design

Time: 3 hrs.

Max. Marks:100

Note: Answer FIVE full questions, selecting at least TWO questions from each part.

PART – A

- 1 a. Explain: i) Embedded system, ii) Hard RTS, iii) Watch Dog Timer, with an example for each. (06 Marks)
- b. With a block diagram, explain briefly the various components in a microprocessor based embedded system. (06 Marks)
- c. Differentiate between the two design approaches for an embedded system development. Explain the various stages with a flow diagram. (08 Marks)
- 2 a. Compare:
 - i) Big Endian and Little Endian formats. (06 Marks)
 - ii) RISC and CISC registers. (06 Marks)
 - iii) Truncation and rounding errors. (06 Marks)
- b. Explain direct and register indirect addressing modes with diagrams. Also write the timing diagram for a serial write operation with an 8 bit register. (06 Marks)
- c. Write the block diagram of RTN model for a microprocessor data path and memory interface. Also explain fetch, execute and next control operations with RTL instructions. (08 Marks)
- 3 a. Explain the internal diagram of SRAM and write the timing diagram for read operation. (06 Marks)
- b. Explain associative mapping cache implementation. (06 Marks)
- c. Write the inside and outside diagrams for DRAM along with read and write operations. Also explain refresh operation. (08 Marks)
- 4 a. Write the flow diagrams for waterfall and V life cycle models and briefly explain Waterfall steps. (06 Marks)
- b. Explain the characterizing and identifying the requirements of a system with respect to a digital counter. (06 Marks)
- c. Write the hardware architecture and data and control flow diagram of a counter system and explain briefly the flow diagram. (08 Marks)

PART – B

- 5 a. Differentiate between:
 - i) Program and process; (06 Marks)
 - ii) Processes and threads;
 - iii) Lightweight and heavy weight threads
- b. Describe:
 - i) Reentrant code, (06 Marks)
 - ii) Foreground/background system,
 - iii) Multithreading system.
- c. Describe the task state transition with a diagram and TCB structures. Explain the function of the scheduler and also dispatcher. (08 Marks)

- 6 a. Explain any 6 functions of an operating system in brief. (06 Marks)
b. Describe virtual model and high level model for OS architectures. (06 Marks)
c. Write the algorithm for a simple OS Kernel, using C language notation for 3 asynchronous tasks using TCBs only. The 3 tasks use a common data buffer for read, increment and display operations. (08 Marks)
- 7 a. Write the Amdahl's law limitation for performance improvement/optimization. Consider a system with the following characteristics.
i) The task to be improved takes 200 time units and the goal is to reduce the execution time to 160 time units. The algorithm under consideration takes 80 time units. Determine the unknown parameter value in the equation and write the inference.
ii) If the goal is to reduce the execution time to 100 time units for the values in case(i), then determine the value unknown parameter value in the equation and write the inference. (06 Marks)
- b. Write a 'C' function to determine the sum of the elements in an array and analyze it line by line for its time complexity (06 Marks)
c. Explain the Big-O notation used for comparing the algorithms, common bounds used with a table, graph and rules used for Big-O arithmetic. (08 Marks)
- 8 a. Write and analyze a linear search algorithm for its time complexity. (06 Marks)
b. The operation to be performed is (i) $c = a + b$, (ii) $c = d + e$ if $a == b$ else $c = d - e$. Write the C language construct and assembly language statements for the above 2 cases separately and calculate the total time required if PUSH/POP takes 800 nsec, arithmetic operation/load/store/cmp takes 400 nsec and the conditional/unconditional branch takes 700 nsec. (06 Marks)
c. Describe memory loading with equation, figure and an example. (08 Marks)

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Eighth Semester B.E. Degree Examination, Dec.2013/Jan.2014

Embedded System Design

Time: 3 hrs.

Max. Marks:100

Note: Answer FIVE full questions, selecting at least TWO questions from each part.

PART – A

1.
 - a. List a pair of design metrics that may compete with one another, providing an intuitive explanation of the reason behind the competition. (06 Marks)
 - b. What is marked window? Derive the percentage revenue loss equation for any rise angle, rather than just for 45 degrees. (08 Marks)
 - c. For a particular product, you determine the NRE cost and unit cost to be the following for the three listed IC technologies:
 FBGA: (\$10,000, \$50), ASIC: (\$50,000, \$10), VLSI: (\$200,000, \$5).
 Determine precise volumes for which each technology yields the lowest total cost. (06 Marks)

2.
 - a. List and define three main design technologies. How are the benefits of using each of three different design technologies helpful to designers? (06 Marks)
 - b. What is single-purpose processor? What are the benefits of choosing a single-purpose processor over the general purpose processor? (04 Marks)
 - c. Design soda machine controller, given that soda costs 75 cents and your machine accepts quarters only. Draw the block box view, come with a state diagram and the state table, minimize the logic and then draw the final circuit. (10 Marks)

3.
 - a. What is meant by pipelining? And why it is used in instruction execution? (06 Marks)
 - b. Explain in detail the general software design tools that are used by embedded system designers. (06 Marks)
 - c. Distinguish in between timer and counter. (04 Marks)
 - d. Explain in detail the operation and initialization sequence of LCD. (04 Marks)

4.
 - a. Given a 100 MHz crystal-controlled oscillator and a 32-bit and any number of 16-bit terminal-count timers, design a real-time clock that output the date and time down to milliseconds. You can ignore leap years. Draw a diagram and indicate terminal count values for all timers. (06 Marks)
 - b. How to control the speed of DC motor by using PWM? (06 Marks)
 - c. Given an analog input signal whose voltage ranges from -5 to 5V, and 8-bit digital encoding, calculate the correct encoding 1.2V and then trace the successive approximation approach to find the correct encoding. (08 Marks)

PART – B

5.
 - a. What is interrupt latency? And explain the factors affecting it. (06 Marks)
 - b. Explain briefly the operation of round-Robin with interrupts. (06 Marks)
 - c. How to selecting an software architecture for your system and give the characteristics of various software architecture? (08 Marks)

- 6 a. Describe the function of scheduler with suitable transition diagram. (06 Marks)
b. Define semaphore and list of tried-and-true ways to mess up with semaphores. (06 Marks)
c. Explain the role timer function in RTOS. (08 Marks)
- 7* a. Explain in briefly encapsulating semaphores and encapsulating queue. (08 Marks)
b. Compose $1K \times 8$ ROMs into $2K \times 16$ ROM. (06 Marks)
c. What are the four main popular serial protocols? And explain the I²C protocol. (06 Marks)
- 8 a. In embedded system how to saving the memory space and power. (10 Marks)
b. Briefly explain which two rules that is used in interrupt routines in an RTOS. (10 Marks)

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06EC82

Eighth Semester B.E. Degree Examination, June/July 2013

Embedded System Design

Time: 3 hrs.

Max. Marks:100

Note: Answer FIVE full questions, selecting at least TWO questions from each part.

PART – A

- 1
 - a. What is an embedded system? Define the three main characteristics of embedded systems that distinguish such systems from other computing systems. (04 Marks)
 - b. Derive the percentage revenue loss equation for a rise angle of 35° . Compute the percentage revenue loss if the products life time is 10 weeks and the delay in market is 5 weeks. (08 Marks)
 - c. Define the three main IC technologies. What are the benefits of using each of the three different IC technologies? (08 Marks)

- 2
 - a. Write a simple algorithm for finding the greatest common divisor of two numbers. Write the FSMD for this algorithm and explain how it can be optimized and write the optimized FSMD. (10 Marks)
 - b. Design a soda machine controller, given that a soda costs 75 cents and your machine accepts quarters only. Draw a black box view, come up with a state diagram and state table, minimize the logic and then draw the final circuit. (10 Marks)

- 3
 - a. Explain how a stepper motor is controlled using driver. Give relevant hardware and software details. (08 Marks)
 - b. The analog input range for an 8 bit ADC is from -2.5 V to +7.5 V. Determine the resolution of ADC and digital output in hexadecimal when the input voltage is 1.2 V. Trace successive approximation steps and show the binary output of the ADC. (08 Marks)
 - c. A watchdog timer that uses two cascaded 16 bit up counters is connected to an 11.981 MHz oscillator. A timeout should occur if the function watchdog_reset is not called within 5 minutes. What value should be loaded into the upcounter pair when the function is called? (04 Marks)

- 4
 - a. Describe fully associative cache mapping technique. (06 Marks)
 - b. Given the following three cache designs, find the one with the best performance by calculating the average cost of access. Show all calculations:
 - i) 4 K byte, 8-way set associative cache with a 6% miss rate; cache hit costs one cycle, cache miss costs 12 cycles.
 - ii) 8 K byte, 4-way set associative cache with a 4% miss rate; cache hit costs two cycles, cache miss costs 12 cycles.
 - iii) 16 K byte, 2-way set associative cache with a 2% miss rate; cache hit costs three cycles, cache miss costs 12 cycles. (08 Marks)
 - c. With a neat diagram, explain the advanced RAM architecture. Also explain how this is extended to improve the performance through synchronous DRAM. (06 Marks)

Important Note : 1. On completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages.
2. Any revealing of identification, appeal to evaluator and/or equations written eg. $42+8=50$, will be treated as malpractice.

PART - B

- 5 a. Describe shared data problem with an example. Show how disable/enable interrupt can be used for solving this problem. (10 Marks)
- b. What is interrupt latency? What factors affecting it? (04 Marks)
- c. Consider three processes with high, medium and low priorities respectively require an execution time of 150 μ sec. 250 μ sec and 350 μ sec. If the interrupts are disabled for 200 μ sec and the deadline for the low priority process is 850 μ sec, determine its worst case interrupt latency. Can it meet the deadline, if the other two interrupts occur? Illustrate with a timing diagram. (06 Marks)
- 6 a. What are semaphores? Explain the semaphore problems in RTOS. (07 Marks)
- b. Explain the RTOS functions "take semaphore" and "release semaphore" with an example. (06 Marks)
- c. What is a task? Explain the three different task states. (07 Marks)
- 7 a. Describe the two rules that an RTOS environment must flow for interrupt routines. (08 Marks)
- b. Explain the advantages and disadvantages of using larger number of tasks in RTOS. (06 Marks)
- c. Identify the bug in the following program and explain:
- ```

Void Task1(void)
{
 :
 :
 VcountErrors (a);
 :
 :
}
Void Task 2(Void)
{
 :
 :
 VcountErrors (11);
 :
 :
}
Static int cErrors ;
Void VcountErrors (int CNew Errors)
{
 CErrors += CNewErrors ;
}

```
- (06 Marks)
- 8 a. Explain "encapsulating semaphores" with an algorithm. (08 Marks)
- b. Explain the methods to save code space and methods to save power. (08 Marks)
- c. What is an event? Explain the three standard features of it. (04 Marks)

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**Eighth Semester B.E. Degree Examination, December 2012**  
**Embedded System Design**

Time: 3 hrs.

Max. Marks:100

**Note: Answer FIVE full questions, selecting  
at least TWO questions from each part.**

**PART – A**

1. a. What are the characteristics of an embedded system? List the design metrics of such a system. (08 Marks)
- b. Compare three processor technologies, along with block diagrams. (08 Marks)
- c. The design of a Disk drive has an NRE cost of \$100,000 and a unit cost of \$20. How much we have to add, to the cost of each product, to cover the NRE cost, assuming that the number of units sold are i) 100 units ii) 10,000 units. What is the total unit cost? (04 Marks)
2. a. Explain RT-level components. (06 Marks)
- b. Explain various steps involved in designing single purpose processor. (06 Marks)
- c. Explain in various events that takes place when a processor executes an instruction. How pipelining improves the execution speed? (08 Marks)
3. a. Explain how DC motor is controlled, using PWM? Assuming an 8-bit up-counter, calculate the count to be loaded in cycle-high register to get pulses of 75% duty-cycle. (08 Marks)
- b. Explain how serial communication is achieved using UART. (04 Marks)
- c. Write necessary hardware and function-pseudocode to
  - i) send control word, to initialize LCD display
  - ii) send a character to display on LCD. (08 Marks)
4. a. Explain flash memory, SRAM, PSRAM and OTP ROM, highlighting their features. (08 Marks)
- b. What is cache memory? Explain how it helps in improving the speed of execution. (06 Marks)
- c. Explain the protocols I<sup>2</sup>C and IEEE 802.11. (06 Marks)

**PART – B**

5. a. Explain how interrupt works in micro-processor. With an example, explain the classic shared data problems, when data is shared between an interrupt and a task. (08 Marks)
- b. What is interrupt latency? What are the factors affecting it? (04 Marks)
- c. Explain with example, Round-Robin architecture. What are its limitations? How do you overcome the limitations of RR architecture. (08 Marks)
6. a. List the characteristics of four software architectures of embedded system software. (08 Marks)
- b. Explain the following with respect to tasks in RTOS-based embedded system:
  - i) Task status
  - ii) Task data. (12 Marks)
7. a. Explain the concept of semaphores. Discuss how it helps in solving shared data problem in embedded system. (08 Marks)
- b. Briefly explain the two rules that the interrupt routines in an RTOS environment must follow. (04 Marks)
- c. Explain the working of message Ques and compare it with pipes. (08 Marks)
8. a. What are encapsulating semaphores? Specify their need with an example. (08 Marks)
- b. Explain the methods to save power and memory. (08 Marks)
- c. Write a brief note on hardware-software co-design aspects in embedded system. (04 Marks)

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06EC82

**Eighth Semester B.E. Degree Examination, June 2012**  
**Embedded System Design**

Time: 3 hrs.

Max. Marks:100

**Note: Answer FIVE full questions, selecting  
at least TWO questions from each part.**

**PART – A**

- 1
  - a. What is an embedded system? Why is it so hard to define? (04 Marks)
  - b. Define time-to-market and NRE cost matrices? The life time of a product is 58 weeks. If the product is delayed by 5 weeks, determine the percentage revenue loss? Determine the per product cost if NRE cost is Rs.500000.00 and unit cost is Rs.8000.00 and company produces 6000 units of that product. (08 Marks)
  - c. Explain how the top-down design process improves the productivity. (08 Marks)
  
- 2
  - a. Explain the purpose of controller and datapath in a single purpose processor. (04 Marks)
  - b. Write a simple algorithm to find GCD of two integer numbers. Write FSM D for this algorithm and explain how it can be optimized. Also write its optimized FSM D. (08 Marks)
  - c. Explain in brief, standard software development process used in embedded system. (08 Marks)
  
- 3
  - a. What is watch-dog timer? What is its use? A 16-bit timer operates at a clock frequency of 20 MHz. Determine the resolution and range of this timer. If a ÷ 4 prescaler is also used, what is the range and resolution of this design? (06 Marks)
  - b. Highlight the advantages of using data in digital form over its analog form. Explain the working of successive approximation type of analog to digital converter, with an example. (10 Marks)
  - c. Explain the features of flash memory and DRAM. (04 Marks)
  
- 4
  - a. Explain in brief, the memory hierarchy and cache operation. Given the following three cache designs, find the one with the best performance, by calculating the average cost of access.
    - i) 4 kbytes, 8-way set associative cache with 6% miss rate. Cache hit costs 1-cycle, cache miss costs 12-cycles.
    - ii) 8 kbytes, 4-way set associative cache with 4% miss rate. Cache hit costs 2-cycles, cache miss costs 12-cycles.
    - iii) 16 kbytes, 2-way set associative cache with 2% miss rate. Cache hit costs 3-cycles, cache miss costs 12-cycles. (10 Marks)
  - b. Design a 2k×16 ROM using 1k×8 ROM using an address decoder. (04 Marks)
  - c. Write the features of USB and IEEE 802.11 protocol. (06 Marks)

Important Note : 1. On completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages.  
2. Any revealing of identification, appeal to evaluator and /or equations written eg, 42+8 = 50, will be treated as malpractice.



**PART – B**

- 5 a. With an example, explain shared data problem. Also explain how an interrupt facility can solve this shared data problem. (10 Marks)
- b. Define interrupt latency. Mention the factors that affects interrupt latency. (04 Marks)
- c. Explain in brief, Function-Queue-Scheduling architecture. (06 Marks)
- 6 a. Briefly compare the methods for intertask communication. (10 Marks)
- b. Explain in brief, three different states of task in RTOS. (05 Marks)
- c. Briefly compare the three methods of protecting shared data. (05 Marks)
- 7 a. What are the two rules, that interrupt routines in most RTOS environment must follow, that do not apply to task codes? (05 Marks)
- b. Illustrate with suitable examples and explain what happens when each rule of question no.7a is violated. (15 Marks)
- 8 a. With suitable example, explain encapsulating semaphores. (08 Marks)
- b. Briefly explain any six problems with semaphores. (07 Marks)
- c. Give the hard real-time scheduling considerations. (05 Marks)

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**Eighth Semester B.E. Degree Examination, December 2011**  
**Embedded System Design**

Time: 3 hrs.

Max. Marks:100

**Note: Answer any FIVE full questions, selecting  
at least TWO questions from each part.**

**PART - A**

- 1 a. What is market window? Why is it important for products to reach the market early in window? Justify. (08 Marks)
- b. Explain how the top-down design process improves the productivity. (06 Marks)
- c. Using the revenue model of Fig.Q1(c), derive the percentage revenue loss equation for any rise angle, rather than just for 45 degrees. (06 Marks)

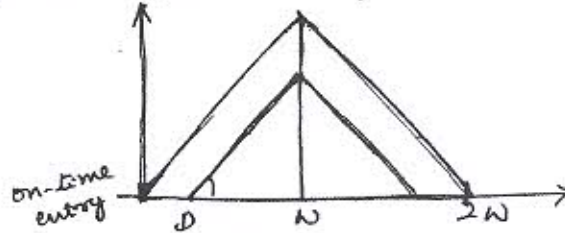


Fig.Q1(c)

- 2 a. Write a simple algorithm for finding the GCD of two integer numbers. Write the FSM for this algorithm. Explain how it can be optimized. Write the optimized FSM and its advantages. (10 Marks)
- b. Briefly explain the purpose of the data path and controller, in a single purpose processor. (10 Marks)
- 3 a. Explain how stepper is controlled using driver. Give relevant hardware and software details. (10 Marks)
- b. In successive approximation, ADC, calculate the correct encoding of 5V, given an analog signal whose voltage ranges from 0 to 15V and a 8-bit digital encoding. Also, determine the resolution of the ADC. (10 Marks)
- 4 a. What is memory hierarchy? How does the cache operate? Discuss the cache mapping technique. List its merits and demerits. (10 Marks)
- b. Describe the I<sup>2</sup>C and IEEE 802.11 protocols. (10 Marks)

**PART - B**

- 5 a. Explain how the interrupt works in a microprocessor. With an example, explain the classic shared data problem, when the data is shared between an interrupt and a task. (10 Marks)
- b. Explain the real time OS architecture. (05 Marks)
- c. What is the interrupt latency? What factors affect it? (05 Marks)
- 6 a. Explain with an example, how round robin architecture works. What is its limitation? (10 Marks)
- b. What are the three different states of task in RTOS? How is the state of each task tracked? (05 Marks)
- c. How does a typically RTOS binary semaphore works? Explain. (05 Marks)
- 7 a. Mention the two rules of interrupt routine in an RTOS environment. With an example, briefly explain, what happens when each rule is violated. (15 Marks)
- b. Compare characteristics of the four software architectures for scheduling. (05 Marks)
- 8 a. Illustrate with suitable examples, the problems of 'delay embrace' and 'priority inversion' (12 Marks)
- b. Explain the methods to solve the memory space and methods to save power. (08 Marks)

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Important Note : 1. On completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages.  
2. Any revealing of identification, appeal to evaluator and/or equations written eg, 42+8 = 50, will be treated as malpractice.



**Eighth Semester B.E. Degree Examination, June/July 2011**  
**Embedded System Design**

Time: 3 hrs.

Max. Marks:100

**Note: Answer FIVE full questions selecting  
at least TWO questions from each part.**

**PART - A**

- 1 a. What is a design metric? Mention the design metric and explain them. (10 Marks)  
 b. Derive an equation for percentage revenue loss for any rise angle rather than just for 45 degrees. (10 Marks)
- 2 a. Design a single-purpose processor that outputs Fibonacci numbers up to 'n' places. Start with a function computing the designed result and translate it into a state diagram. (10 Marks)  
 b. Design a combinatorial logic for y and z where y is 1, if a is 1, or 'b' and 'c' are 1 and z is 1 if 'b' or 'c' is 1, but not both (or a, b and c are all 1). (10 Marks)
- 3 a. What is watchdog timer? Explain ATM timeout using a watchdog timer. (10 Marks)  
 b. Describe the working of PWM unit with timing diagrams. How can it be used for speed control of DC motor? (10 Marks)
- 4 a. Explain the features of flash memory, SRAM and OTP ROM. (06 Marks)  
 b. Explain memory hierarchy and cache operation. (08 Marks)  
 c. Design a 8k×8 ROM using 1k×8 ROM using an address decoder. (06 Marks)

**PART - B**

- 5 a. Explain shared data problem with an example, show how interrupt facility can be used for solving the problem. (10 Marks)  
 b. Explain interrupt handling procedure, context switching and critical section. (10 Marks)
- 6 a. Briefly compare the methods for intertask communication. (10 Marks)  
 b. Give drawbacks of 'malloc' and 'free' library functions of C in real time systems. Explain getbuf and regbuf using program code. (10 Marks)
- 7 a. Explain interrupt routines in RTOS environment. (10 Marks)  
 b. What is meant by encapsulating the semaphores? Bring out the need for it. (10 Marks)
- 8 a. Explain how memory space can be saved in hard real time scheduling with an example. (10 Marks)  
 b. Discuss any five problems with semaphores. (10 Marks)

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EC835

## Eighth Semester B.E. Degree Examination, June/July 2011 Embedded System Design

Time: 3 hrs.

Max. Marks:100

**Note:1. Answer any FIVE full questions.  
2. Missing data may be suitably assumed.**

- 1 a. Write a simple algorithm for finding GCD of two integer numbers. Write FSM D for this algorithm and explain how it can be optimized and write the optimized FSM D. (08 Marks)  
b. Define time to market and NRE cost metrics. The life time of a product is 58 weeks. If the product is delayed by 6 weeks, determine the percentage revenue loss. Determine the per product cost if NRE cost is Rs.400000 and unit cost is Rs.8000 and company produces 5000 units of that product. (08 Marks)  
c. Explain the 3 main processor technologies that are used with embedded system. Also give the merits of each. (04 Marks)
- 2 a. What is operating system? Explain a scheme to invoke system call. (08 Marks)  
b. With code, explain how the parallel port of a PC can be used to perform digital I/O. (08 Marks)  
c. Explain the concept of pipelining. (04 Marks)
- 3 a. With diagram explain, i) Timer / Counter ii) Timer with terminal count  
iii) Timer with prescaler iv) 16 bit timer. (08 Marks)  
b. Implement ATM time out using watch dog timer. Give timer structure, main pseudo-code and watch dog reset routine. (08 Marks)  
c. Give the ISA bus protocol timing for, i) Read bus ii) Write bus. (04 Marks)
- 4 a. Give a scheme and software to control the stepper motor directly. (08 Marks)  
b. Explain the cache mapping techniques. (08 Marks)  
c. Explain CAN protocol. (04 Marks)
- 5 a. What is shared data problem? Explain with example. Give the solutions to solve this problem. (08 Marks)  
b. Mention the factors that effects interrupt latency. (04 Marks)  
c. With example, give alternatives to disabling interrupts. (08 Marks)
- 6 a. Give the characteristics of various software architectures. (08 Marks)  
b. With diagram, explain semaphore problems and priority inversion. (08 Marks)  
c. Explain : i) Counting semaphores ii) Resource semaphores. (04 Marks)
- 7 a. Explain the two rules that interrupt routines in most RTOS must follow that do not apply to task code. (08 Marks)  
b. With example, explain encapsulating semaphores and ques. (08 Marks)  
c. Give the hard real time scheduling considerations. (04 Marks)
- 8 Write notes on the following:  
a. Saving memory space.  
b. Events  
c. I<sup>2</sup>C law  
d. Parallel protocols. (20 Marks)



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EC835

**Eighth Semester B.E. Degree Examination, December 2010**  
**Embedded System Design**

Time: 3 hrs.

Max. Marks:100

**Note: 1. Answer any FIVE full questions.**  
**2. Standard notations are used.**  
**3. Missing data may be suitably assumed.**

- 1
  - a. What are the characteristics of an embedded system design? List the design metrics used to compare them. (07 Marks)
  - b. Determine the revenue loss, if the product's lifetime is 74 weeks and the delay in the market is 6 weeks. Derive the formula used for the calculation. (07 Marks)
  - c. For a particular product, determine the NRE cost and unit cost to be the following for the three listed IC technologies:  
 FPGA (\$10000, \$50): ASIC (\$50000, \$10)  
 VLSI (\$200000, \$5)  
 Determine the precise volumes for which each technology yields the lowest total cost. (06 Marks)
- 2
  - a. Develop an efficient algorithm for GCD. Convert it to FSM and show the optimized FSM.
  - b. With a neat diagram, explain the architecture of a general purpose processor. (10 Marks)
- 3
  - a. Define the following: (04 Marks)  
 i) Cross compiler      ii) Emulator      iii) Debugger      iv) In circuit simulator
  - b. Differentiate between: (06 Marks)  
 i) Single purpose and general purpose processors  
 ii) Harvard and von-Neumann architecture
  - c. With a neat diagram, explain how the pulse width modulator works. What are the considerations in selecting the clock, the prescaler and the counter? Assuming an 8-bit up counter, calculate the count to be loaded in the 'cycle-high' register to get pulses of duty cycle 75%. (10 Marks)
- 4
  - a. Given an analog input signal whose voltage ranges from 0 to 5 v and an 8-bit digital encoding, calculate the correct encoding for 3.5 v and then trace the successive approximation approach to find the correct encoding. (08 Marks)
  - b. What is cache mapping? Explain the direct mapping techniques for cache. (08 Marks)
  - c. Explain the terms write ability and storage permanence. (04 Marks)
- 5
  - a. Explain two level multibus architecture, with a neat diagram. (06 Marks)
  - b. Compose 1K × 8 ROMs into 2K × 16 ROM. (06 Marks)
  - c. Given the following three cache designs, find the one with the best performance, by calculating the average cost of access. Show all calculations.
    - i) 4K byte, 8-way-set associative cache, with a 6% miss rate; cache hit costs one cycle, cache miss costs 12 cycles
    - ii) 8K byte, 4-way-set associative cache with a 4% miss rate; cache hit costs 2 cycles, cache miss costs 12 cycles
    - iii) 16K byte, 2-way-set associative cache with a 2% miss rate; cache hit costs 3cycles, cache miss costs 12 cycles. (08 Marks)

Important Note : 1. On completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages.  
 2. Any revealing of identification, appeal to evaluator and /or equations written eg, 42+8 = 50, will be treated as malpractice.

- 6 a. What is interrupt latency? What are the factors affecting it? (08 Marks)  
b. Explain with an example, how the Round-Robin architecture works. When is it not suitable? (08 Marks)  
c. What is a reentrant function? Give the three rules to decide reentrant functions. (04 Marks)
- 7 a. What is semaphore? Explain RTOS semaphore. (10 Marks)  
b. Differentiate between hard and soft RTOS highlighting the advantages and disadvantages of each. (06 Marks)  
c. Explain 'deadly embrace'. (04 Marks)
- 8 a. What is an event? Give three standard features of an event. (05 Marks)  
b. Give a comparison of methods for inter task communication. (04 Marks)  
c. Explain the two rules, that the interrupt routines must follow, in RTOS environment. What is the effect of blocking on interrupts? Explain with a diagram. (08 Marks)  
d. Explain the role of timer function in RTOS. (03 Marks)

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Master Set

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06EC82

**Eighth Semester B.E. Degree Examination, May/June 2010**  
**Embedded System Design**

Time: 3 hrs.

Max. Marks:100

**Note: Answer any FIVE full questions, selecting  
at least TWO questions from each part.**

**PART – A**

- 1 a. Mention the characteristics and briefly list the design metrics of an embedded system. (08 Marks)
- b. Determine the percentage of revenue loss if the products life time is 86 weeks and the delay in the market is 8 weeks. Derive the formula used for this calculation. (06 Marks)
- c. Explain how the top-down design process improves the productivity. (06 Marks)
- 2 a. Briefly explain the purpose of the data path and controller in a single purpose processor. (06 Marks)
- b. Write an efficient algorithm for finding the GCD of two integer numbers. Also explain how the FSMD for this can be optimized. (08 Marks)
- c. Explain various addressing modes that are commonly used by processors, with an example. (06 Marks)
- 3 a. Explain how UART is used for communication. List its advantages. (08 Marks)
- b. What is a watch dog timer? List its uses. A 16 bit timer operates at a clock frequency of 12 MHz. Determine the resolution and range of this timer. (06 Marks)
- c. The analog input range for a 8-bit ADC is from -2.5V to 8.5V. Determine the resolution of ADC and digital output in hexadecimal, when the input voltage is 1.2V. Trace successive approximation steps and show the binary output of the ADC. (06 Marks)
- 4 a. What is memory hierarchy? How does the cache operate? Discuss the cache mapping techniques. List their merits and demerits. (10 Marks)
- b. Briefly explain OTPROM, EEPROM, RDRAM and FPM DRAM. (10 Marks)

**PART – B**

- 5 a. Explain the need for interrupts in processors and mention briefly the various events that take place when a processor is interrupted. (10 Marks)
- b. Explain the problems of shared-data interrupts and suggest the solution to solve the problems. (10 Marks)
- 6 a. Explain with an example, how the Round-Robin architecture works. What is its limitation? (12 Marks)
- b. List the characteristics of four software architectures available for building embedded software. (08 Marks)
- 7 a. Mention the two rules of interrupt routines in an RTOS environment. With an example, briefly explain, what happens when each rule is violated. (15 Marks)
- b. Describe the use of message queues. (05 Marks)
- 8 a. What is meant by encapsulating the semaphores? Bring out the need for it. (08 Marks)
- b. Explain any six problems of semaphores. (06 Marks)
- c. Explain the methods to solve memory space and methods to save power. (06 Marks)

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Important Note : 1. On completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages.  
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EC835

**Eighth Semester B.E. Degree Examination, May/June 2010**  
**Embedded System Design**

Time: 3 hrs.

Max. Marks:100

**Note: Answer any FIVE full questions.**

- 1
  - a. Define an Embedded system. Explain any three important characteristics of an embedded system. (06 Marks)
  - b. What is a Watchdog Timer? Why it is so called? Explain its role in the design of any embedded system. (06 Marks)
  - c. Determine the percentage revenue loss if the product life time is 74 weeks and the delay in the market is 6 weeks. Derive the formula used. (08 Marks)
  
- 2
  - a. Explain the concept of 'datapath' as applied to an embedded system. Give an example. (06 Marks)
  - b. Explain the role of a Finite State Machine (FSM) model in the design of an embedded system using a suitable example. (06 Marks)
  - c. Assume an 8 bit encoding of input voltage in the range  $-5V$  to  $+5V$ . Calculate the encoding for 1.2V and trace the successive approximation approach to find the correct encoding. What is the resolution of the conversion? (08 Marks)
  
- 3
  - a. Explain the steps involved in designing a general purpose processor. (06 Marks)
  - b. Explain the concept of PWM speed control circuit as applied to an embedded system. (06 Marks)
  - c. Define the following : i) Assembler ii) Cross compiler iii) Emulator iv) Simulator. (08 Marks)
  
- 4
  - a. Differentiate between : i) PSRAM and NVRAM ii) SRAM and DRAM iii) FLASH and EPROM. (06 Marks)
  - b. Briefly describe the principles used in three replacement policies normally employed during cache memory operation. (06 Marks)
  - c. In a hierarchy design of memory, the cache miss rate is 15%, cost of memory access is 20 cycles and cost of cache access is 2 cycles. Determine the average cost of access. (08 Marks)
  
- 5
  - a. Show an interface of  $2k \times 16$ ROM from  $1k \times 8$ ROM. Explain the decoding logic used. (06 Marks)
  - b. Explain the features of the following bus architecture : i) CAN bus ii) IEEE – 802.11. (06 Marks)
  - c. What is multi – level bus architecture? Explain its need and also the reasons to improve the processor performance by this architecture. (08 Marks)
  
- 6
  - a. What is interrupt latency? Explain the factors affecting it. (06 Marks)
  - b. Describe Round Robin architecture with an example. (06 Marks)
  - c. Define semaphore and critical sections as applied to real time operating system. (08 Marks)
  
- 7
  - a. Describe the function of a scheduler with a suitable transition diagram. (06 Marks)
  - b. Explain the use of message queues with an example. (06 Marks)
  - c. Explain the role of timer function in RTOS. (08 Marks)
  
- 8
  - a. Discuss briefly Hard Real time scheduling considerations. (06 Marks)
  - b. What is meant by encapsulating a semaphores? Mention its applications. (06 Marks)
  - c. Write a brief note on : i) Deadly Embrace ii) Priority Inversion. (08 Marks)

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# 2002 SCHEME

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EC835

## Eighth Semester B.E. Degree Examination, June-July 2009

### Embedded System Design

Time: 3 hrs.

Max. Marks:100

**Note: Answer any FIVE full questions.**

- 1 a. Derive the equation for percentage revenue loss for any market rise angle  $\theta$ . A product was delayed by 4 weeks in releasing to market. The peak revenue for the product for on-time entry to market would occur after 20 weeks for a market rise angle of  $45^\circ$ . Determine the percentage revenue loss. **(08 Marks)**
- b. Compare GPP, SPP and ASSP along with their block diagrams and any two differences. **(06 Marks)**
- c. Given the following details, draw the graphs of total cost Vs volume and per-product cost Vs volume. Make a table for volumes 400, 800, 1200, 1600, 2000 and 2400 for all the three technologies.

|           | Technology A | Technology B | Technology C |
|-----------|--------------|--------------|--------------|
| NRE cost  | \$ 2,000     | \$ 30,000    | \$100,000    |
| Unit cost | \$ 100       | \$ 30        | \$ 2         |

**(06 Marks)**

- 2 a. Write an algorithm for GCD with more time complexity and write the FSM and also determine the total number of steps required for GCD (42, 8) in this case. **(08 Marks)**
- b. Explain pipelining for instruction execution with 5 stages. Determine the speed up, if 200 instructions are executed at a clock frequency of 10 MHz in this pipelined processor. **(06 Marks)**
- c. Explain the terms : Dhrystone Benchmark, Linker and Moore's law. **(06 Marks)**
- 3 a. Explain the working of stepper motor using a driver. **(08 Marks)**
- b. Describe register, relative and direct addressing modes in a processor with an example for each. **(06 Marks)**
- c. Determine the range and resolution of a 16 bit timer which operates at a clock frequency of 10 MHz and generates an overflow signal when it reaches FFFF. Calculate the terminal count value for measuring a 3 msec time interval. What is the minimum division needed in a prescaler for measuring 100 msec? **(06 Marks)**
- 4 a. The analog input range for an 8 bit ADC is  $-5V$  to  $+5V$ . Determine the resolution of this ADC and also the digital output in binary when the input is  $-2V$  using formula. Also trace the successive approximation steps for verification. Write it in a tabular form with necessary columns. **(08 Marks)**
- b. Describe the working of a PWM unit with a circuit and waveforms. **(06 Marks)**
- c. Explain the features of flash memory, SRAM and OTP ROM. **(06 Marks)**
- 5 a. Describe set associative cache mapping technique. What are its merits and demerits? **(08 Marks)**
- b. Compose a  $4 K \times 32$  bit ROM using a required number of  $2 K \times 8$  bit ROMs. Show the connection diagram and write the memory map. **(06 Marks)**
- c. Write the features of CAN bus, PCI bus and Bluetooth protocol. **(06 Marks)**

- 6 a. Describe shared data problem with an example. Show how disable/ enable interrupt can be used for solving this problem. (08 Marks)
- b. Explain interrupt handling procedure, context switching and critical section. (06 Marks)
- c. Let the minimum interrupt latency in a system be 100  $\mu$ sec and context switching time is negligible. The execution time for high, medium and low priority processes be 200  $\mu$ sec, 400  $\mu$ sec and 600  $\mu$ sec respectively. The deadline for the low priority process be 1000  $\mu$ sec. Is it possible for the low priority process to complete its execution if –  
i) both high and medium processes interrupt it and ii) only high priority process interrupts it?  
Write timing diagrams for both the cases and indicate worst case interrupt latency and total time. (06 Marks)
- 7 a. Describe round robin architecture for digital multi-meter example. (08 Marks)
- b. Explain function queue scheduling. (06 Marks)
- c. Describe the function of a scheduler with a task state transition diagram. (06 Marks)
- 8 a. Describe the use of take semaphore ( ) and release semaphore ( ) with an example. (08 Marks)
- b. Explain any 6 problems with semaphores. (06 Marks)
- c. Describe the use of message queues. (06 Marks)

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EE841

**Eighth Semester B.E. Degree Examination, May/June 08**  
**Embedded Systems**

Time: 3 hrs.

Max. Marks:100

**Note : Answer any FIVE full questions.**

- 1
  - a. What do you understand by system on chip? Why is it needed? Sketch a typical SOC for cellphone and explain the prominent units. (10 Marks)
  - b. Outline the various registers and internal RAM structure of 8051 microcontroller.(10 Marks)
  
- 2
  - a. Explain the various data structures employed to write programs for embedded systems. (10 Marks)
  - b. What are the advantages and disadvantages of RTOS architecture? Give the pseudocode of such an architecture. (10 Marks)
  
- 3
  - a. What are reentrant functions? How do you test a C function for reentrancy? Give examples. (08 Marks)
  - b. What are semaphores and why do you need them? List and explain the various problems associated with semaphores in programming. (12 Marks)
  
- 4
  - a. With the help of a circuit schematic, analyse the operation of unsigned and signed 3-bit DAC. (14 Marks)
  - b. Discuss techniques to generate any complex waveform using a NC and DAC. (06 Marks)
  
- 5
  - a. Give the functional block diagram of a typical ADC system and explain. (06 Marks)
  - b. Discuss the need for sample and hold circuits. (04 Marks)
  - c. Give the flowchart to record digital data from an ADC having 2-channels and containing
    - i) S/H and
    - ii) no S/H
 (10 Marks)
  
- 6
  - a. Illustrate the concept of pull-up and pull-down key interface to 1-bit port. (06 Marks)
  - b. Illustrate the number of keys that can be interfaced to a single 8-bit port by
    - i) Direct
    - ii) Scanned and
    - iii) Multiplexed methods.
 (14 Marks)
  
- 7
  - a. Illustrate H-bridge schematic to run DC motor in either direction. Also discuss the precautions to be taken. (12 Marks)
  - b. List the important signals of RS 232 communication cable. What are its limitations? (08 Marks)
  
- 8
 

Discuss briefly :

  - a. Issues in embedded system design
  - b. Performance design metrics
  - c. Skills required to design embedded system
  - d. Memory interfacing. (20 Marks)

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