Unit 7: Memory

Objectives: At the end of this unit we will be able to understand

- System timing consideration
- Storage / Memory Elements
  - dynamic shift register
  - 1T and 3T dynamic memory
  - 4T dynamic and 6T static CMOS memory
- Array of memory cells

System timing considerations:

- Two phase non-overlapping clock
- ϕ_1 leads ϕ_2
- Bits to be stored are written to register and subsystems on ϕ_1
- Bits or data written are assumed to be settled before ϕ_2
- ϕ_2 signal used to refresh data
- Delays assumed to be less than the intervals between the leading edge of ϕ_1 & ϕ_2
- Bits or data may be read on the next ϕ_1
- There must be atleast one clocked storage element in series with every closed loop signal path

Storage / Memory Elements:

The elements that we will be studying are:

- Dynamic shift register
- 3T dynamic RAM cell
- 1T dynamic memory cell
- Pseudo static RAM / register cell
- 4T dynamic & 6T static memory cell
- JK FF circuit
- D FF circuit

Dynamic shift register:

Circuit diagram: Refer to unit 4(ch 6.5.4)

Power dissipation

- static dissipation is very small
- dynamic power is significant
- dissipation can be reduced by alternate geometry

Volatility

- data storage time is limited to 1msec or less

3T dynamic RAM cell:

Circuit diagram

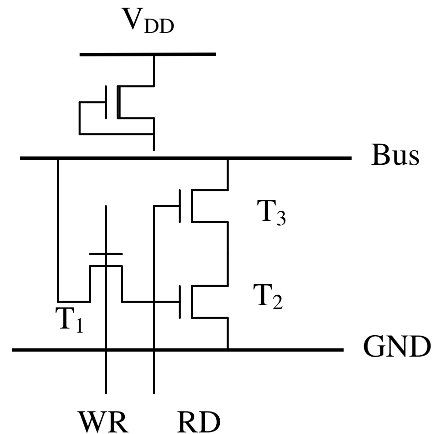

Figure 7.1: 3T Dynamic RAM Cell

Working

- RD = low, bit read from bus through T1, WR = high, logic level on bus sent to Cg of T2, WR = low again
- Bit level is stored in Cg of T2, RD=WR=low
- Stored bit is read by RD = high, bus will be pulled to ground if a 1 was stored else 0 if T2 non-conducting, bus will remain high.

Dissipation

- Static dissipation is nil
- Depends on bus pull-up & on duration of RD signal & switching frequency

Volatility

- Cell is dynamic, data will be there as long as charge remains on Cg of T2

1T dynamic memory cell:

Circuit diagram

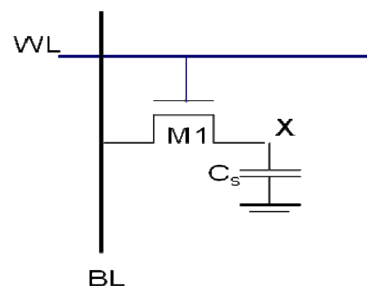

Figure 7.2: 1T Dynamic RAM Cell

Working

- Row select (RS) = high, during write from R/W line Cm is charged
- data is read from Cm by detecting the charge on Cm with RS = high
- cell arrangement is bit complex.
- solution: extend the diffusion area comprising source of pass transistor, but Cd<<< Cgchannel
- another solution : create significant capacitor using poly plate over diffusion area.
- Cm is formed as a 3-plate structure
- with all this careful design is necessary to achieve consistent readability

Dissipation

- no static power, but there must be an allowance for switching energy during read/write

Pseudo static RAM / register cell:

Circuit diagram

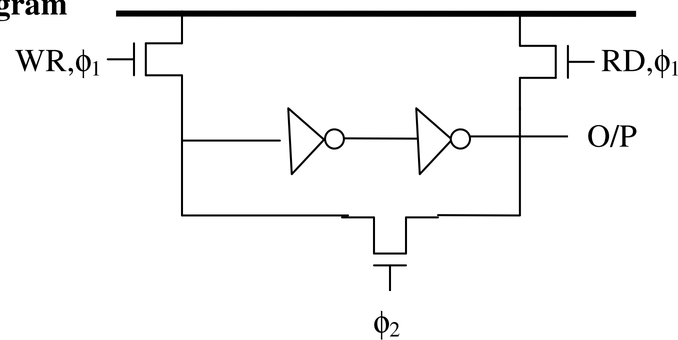

Figure 7.3: nMOS pseudo-static memory Cell

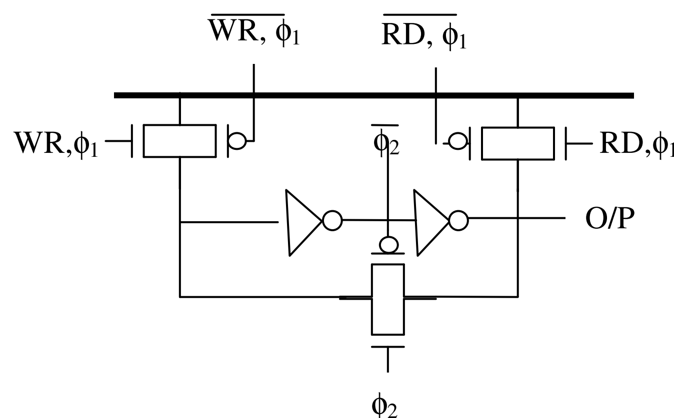

Figure 7.4: CMOS pseudo-static memory Cell

Working

- dynamic RAM need to be refreshed periodically and hence not convenient
- static RAM needs to be designed to hold data indefinitely
- One way is connect 2 inverter stages with a feedback.
- say ϕ_2 to refresh the data every clock cycle
- bit is written on activating the WR line which occurs with ϕ_1 of the clock
- bit on Cg of inverter 1 will produce complemented output at inverter 1 and true at output of inverter 2
- at every ϕ_2 , stored bit is refreshed through the gated feedback path
- stored bit is held till ϕ_2 of clock occurs at time less than the decay time of stored bit
- to read RD along with ϕ_1 is activated

Note:

- WR and RD must be mutually exclusive
- ϕ_2 is used for refreshing, hence no data to be read, if so charge sharing effect, leading to destruction of stored bit
- cells must be stackable, both side-by-side & top to bottom
- allow for other bus lines to run through the cell

4T dynamic & 6T static memory cell:

Circuit diagram

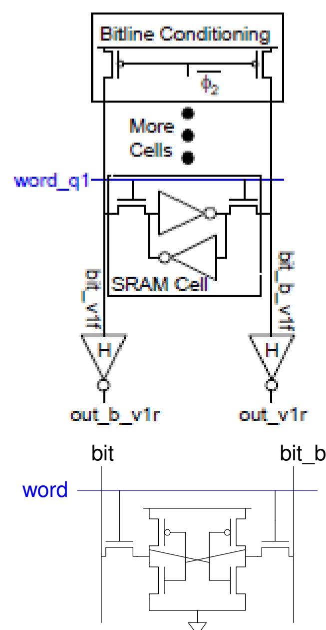

Figure 7.4: Dynamic and static memory cells

Working

- uses 2 buses per bit to store bit and bit'
- both buses are precharged to logic 1 before read or write operation.
- write operation
- read operation

Write operation

- both bit & bit' buses are precharged to VDD with clock ϕ_1 via transistor T5 & T6
- column select line is activated along with ϕ_2
- either bit or bit' line is discharged along the I/O line when carrying a logic 0
- row & column select signals are activated at the same time => bit line states are written in via T3 & T4, stored by T1 & T2 as charge

Read operation

- bit and bit' lines are again precharged to VDD via T5 & T6 during ϕ_1
- if 1 has been stored, T2 ON & T1 OFF
- bit' line will be discharged to VSS via T2
- each cell of RAM array be of minimum size & hence will be the transistors
- implies incapable of sinking large charges quickly

- RAM arrays usually employ some form of sense amplifier
  - T1, T2, T3 & T4 form as flip-flop circuit
  - if sense line to be inactive, state of the bit line reflects the charge present on gate capacitance of T1 & T3
  - current flowing from VDD through an on transistor helps to maintain the state of bit lines